



ICS512 LOCO™ PLL Clock Multiplier

Description

The ICS512 LOCO™ is the most cost effective way to generate a high quality, high frequency clock output and a reference clock from a lower frequency crystal or clock input. The name LOCO stands for LOW Cost Oscillator, as it is designed to replace crystal oscillators in most electronic systems. Using Phase-Locked-Loop (PLL) techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 200 MHz. With a reference output, this chip plus an inexpensive crystal can replace two oscillators.

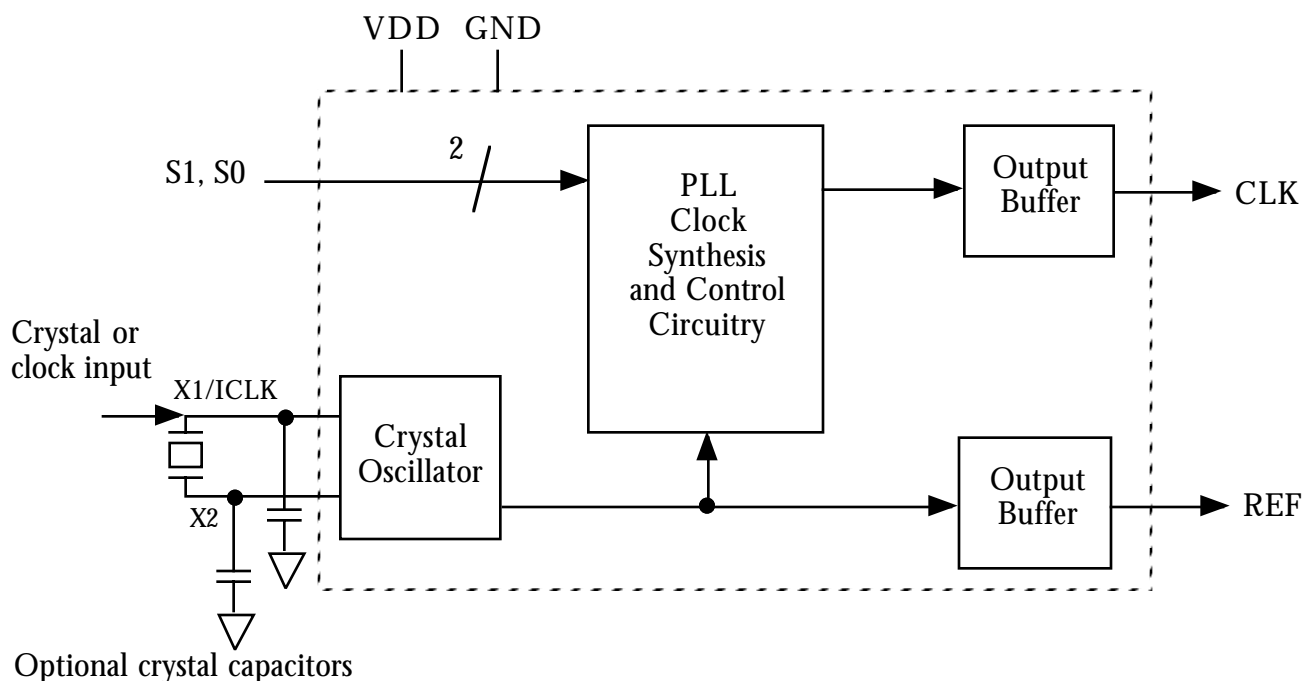
Stored in the chip's ROM is the ability to generate nine different popular multiplication factors, allowing one chip to output many common frequencies (see page 2).

Features

- Packaged as 8 pin SOIC or die
- Upgrade of popular ICS502 with:
 - changed multiplier table
 - higher operating frequencies
- Zero ppm multiplication error
- Easy to cascade with other 5xx series
- Input crystal frequency of 5 - 27 MHz
- Input clock frequency of 2 - 50 MHz
- Output clock frequencies up to 200 MHz
- Compatible with all popular CPUs
- Duty cycle of 45/55 up to 200 MHz
- Mask option for 9 selectable frequencies
- Operating voltages of 3.0 to 5.5V
- Industrial temperature version available
- Advanced, low power CMOS process

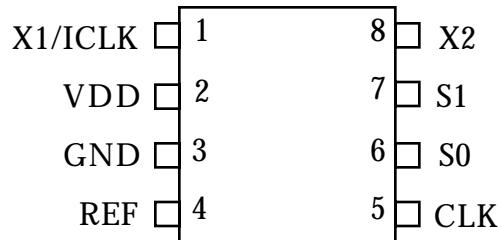


Block Diagram





Pin Assignment



Clock Output Table

| S1 | S0 | CLK |
|----|----|--------------|
| 0 | 0 | 4X input |
| 0 | M | 5.333X input |
| 0 | 1 | 5X input |
| M | 0 | 2.5X input |
| M | M | 2X input |
| M | 1 | 3.333X input |
| 1 | 0 | 6X input |
| 1 | M | 3X input |
| 1 | 1 | 8X input |

0 = connect directly to ground.
 1 = connect directly to VDD.
 M = leave unconnected (floating).

Common Output Frequencies Examples (MHz)

| | | | | | | | | | | | |
|---------------------------|--------------|-----------|-----------|-----------|--------------|-------------|------------|------------|------------|---------------|------------|
| Output | 20 | 24 | 30 | 32 | 33.33 | 37.5 | 40 | 48 | 50 | 60 | 64 |
| Input | 10 | 12 | 10 | 16 | 16.66 | 15 | 10 | 12 | 20 | 10 | 16 |
| Selection (S1, S0) | M, M | M, M | 1, M | M, M | M, M | M, 0 | 0, 0 | 0, 0 | M, 0 | 1, 0 | 0, 0 |
| Output | 66.66 | 72 | 75 | 80 | 83.33 | 90 | 100 | 120 | 125 | 133.33 | 150 |
| Input | 20 | 12 | 25 | 10 | 25 | 15 | 20 | 15 | 25 | 25 | 25 |
| Selection (S1, S0) | M, 1 | 1, 0 | 1, M | 1, 1 | M, 1 | 1, 0 | 0, 1 | 1, 1 | 0, 1 | 0, M | 1, 0 |

Note that all of the above outputs are achieved by using a common, inexpensive 10MHz to 25MHz crystal. Consult ICS on how to achieve other output frequencies.

Pin Descriptions

| Number | Name | Type | Description |
|--------|---------|------|--|
| 1 | X1/ICLK | XI | Crystal connection or clock input. |
| 2 | VDD | P | Connect to +3.3V or +5V. |
| 3 | GND | P | Connect to ground. |
| 4 | REF | O | Buffered crystal oscillator output clock. |
| 5 | CLK | O | Clock output per Table above. |
| 6 | S0 | TI | Multiplier select pin 0. Connect to GND or VDD or float (no connection). |
| 7 | S1 | TI | Multiplier select pin 1. Connect to GND or VDD or float (no connection). |
| 8 | X2 | XO | Crystal connection. Leave unconnected for clock input. |

Key: XI/XO = crystal connections, TI = tri-level input, O = output, P = power supply connection



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Electrical Specifications

| Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---------------------|-----------|----------|-----------|-------|
| ABSOLUTE MAXIMUM RATINGS (stresses beyond these can permanently damage the device) | | | | | |
| Supply Voltage, VDD | Referenced to GND | | | 7 | V |
| Inputs | Referenced to GND | -0.5 | | VDD+0.5 | V |
| Clock Output | Referenced to GND | -0.5 | | VDD+0.5 | V |
| Ambient Operating Temperature | | 0 | | 70 | °C |
| | ICS512MI only | -40 | | 85 | °C |
| Soldering Temperature | Max of 10 seconds | | | 260 | °C |
| Storage temperature | | -65 | | 150 | °C |
| DC CHARACTERISTICS (VDD = 3.3V unless otherwise noted) | | | | | |
| Operating Voltage, VDD | | 3 | | 5.5 | V |
| Input High Voltage, VIH, ICLK only | ICLK (Pin 1) | (VDD/2)+1 | VDD/2 | | V |
| Input Low Voltage, VIL, ICLK only | ICLK (Pin 1) | | VDD/2 | (VDD/2)-1 | V |
| Input High Voltage, VIH | S0, S1 | VDD-0.5 | | | V |
| Input Low Voltage, VIL | S0, S1 | | | 0.5 | V |
| Output High Voltage, VOH, CMOS high | IOH=-8mA | VDD-0.4 | | | V |
| Output High Voltage, VOH | IOH=-12mA | 2.4 | | | V |
| Output Low Voltage, VOL | IOL=12mA | | | 0.4 | V |
| IDD Operating Supply Current, 20 MHz crystal | No Load, 100MHz | | 9 | | mA |
| Short Circuit Current | CLK output | | ±70 | | mA |
| Input Capacitance, S1, S0 | Pins 6, 7 | | 4 | | pF |
| AC CHARACTERISTICS (VDD = 3.3V unless otherwise noted) | | | | | |
| Input Frequency, crystal input | | 5 | | 27 | MHz |
| Input Frequency, clock input | | 2 | | 50 | MHz |
| Output Frequency, VDD = 4.5 to 5.5V Note 1 | 0 to +70 °C | 14 | | 200 | MHz |
| | -40 to +85 °C | 14 | | 160 | MHz |
| Output Frequency, VDD = 3.0 to 3.6V Note 1 | 0 to +70 °C | 14 | | 160 | MHz |
| | -40 to +85 °C | 14 | | 145 | MHz |
| Output Clock Rise Time | 0.8 to 2.0V | | 1 | | ns |
| Output Clock Fall Time | 2.0 to 0.8V | | 1 | | ns |
| Output Clock Duty Cycle | at VDD/2 | 45 | 49 to 51 | 55 | % |
| Absolute Clock Period Jitter | Deviation from mean | | ±200 | | ps |
| One Sigma Clock Period Jitter | | | 80 | | ps |

Note 1: The phase relationship between input and output clocks can change at power up. For a fixed phase relationship, see the ICS570 or the ICS527.

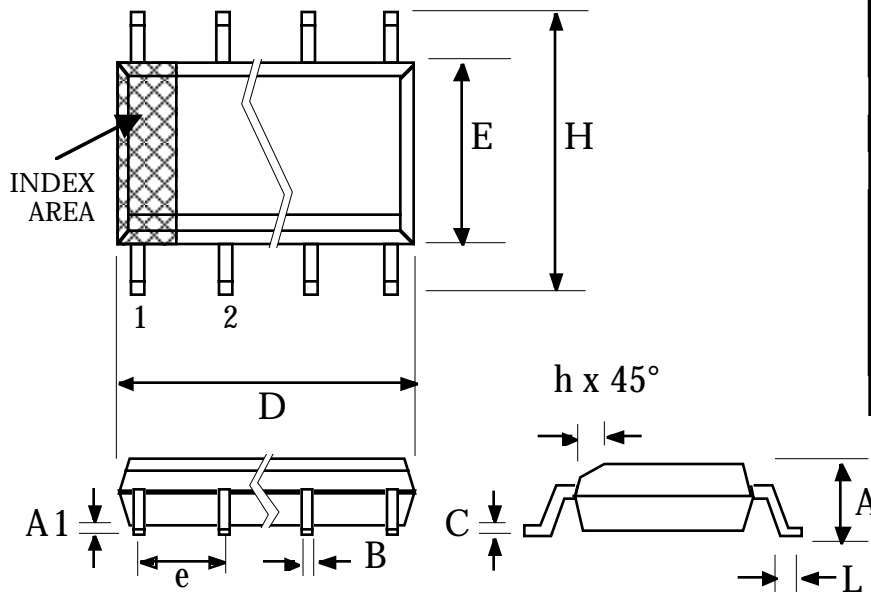


External Components / Crystal Selection

The ICS512 requires a 0.01μF decoupling capacitor to be connected between VDD and GND. It must be connected close to the ICS512 to minimize lead inductance. No external power supply filtering is required for this device. A 33 Ω terminating resistor can be used next to the CLK and REF pins. The total on-chip capacitance is approximately 15 pF, so a parallel resonant, fundamental mode crystal should be used. For crystals with a specified load capacitance greater than 15 pF, crystal capacitors should be connected from each of the pins X1 and X2 to Ground as shown in the Block Diagram on page 1. The value (in pF) of these crystal caps should be = $(C_L - 15) * 2$, where C_L is the crystal load capacitance in pF. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either).

Package Outline and Package Dimensions (For current dimensional specifications, see JEDEC 95.)

8 pin SOIC



| Symbol | Inches | | Millimeters | |
|--------|----------|--------|-------------|------|
| | Min | Max | Min | Max |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.24 |
| B | 0.0130 | 0.0200 | 0.33 | 0.51 |
| C | 0.0075 | 0.0098 | 0.19 | 0.24 |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 |
| e | .050 BSC | | 1.27 BSC | |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 |
| h | 0.0099 | 0.0195 | 0.25 | 0.50 |
| L | 0.0160 | 0.0500 | 0.41 | 1.27 |

Ordering Information

| Part/Order Number | Marking | Package | Temperature |
|-------------------|---------|-----------------------------|---------------|
| ICS512M | ICS512M | 8 pin SOIC | 0 to 70 °C |
| ICS512MT | ICS512M | 8 pin SOIC on tape and reel | 0 to 70 °C |
| ICS512MI | ICS512I | 8 pin SOIC | -40 to +85 °C |
| ICS512MIT | ICS512I | 8 pin SOIC on tape and reel | -40 to +85 °C |

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